



SA[0:19] SA[0:19]  
SD[0:15] SD[0:15]

IRQ[3:5] IRQ[3:5]  
IRQ[9:12] IRQ[9:12]  
IRQ15 IRQ15

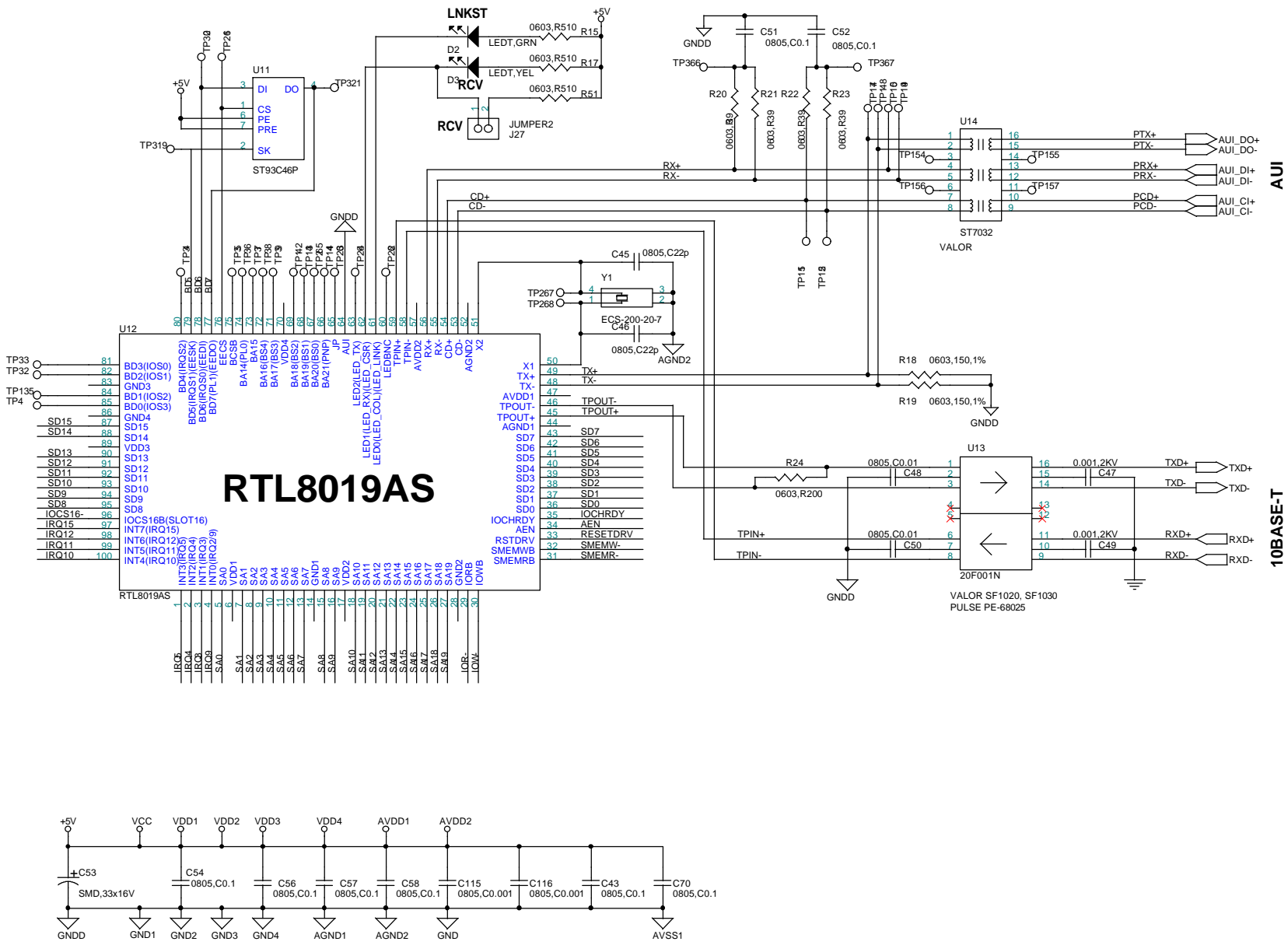
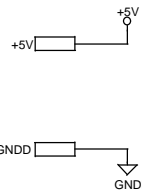
IOCHRDY IOCHRDY  
IOCS16 IOCS16

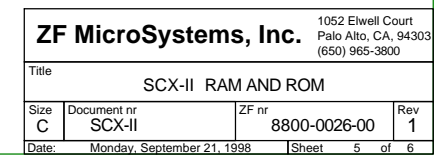
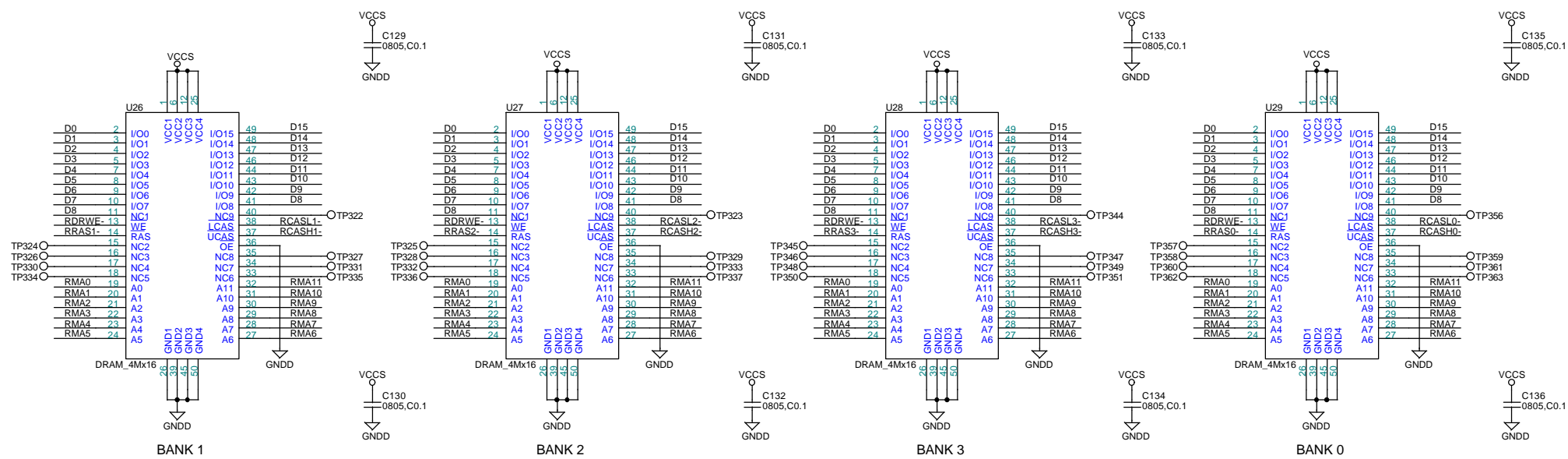
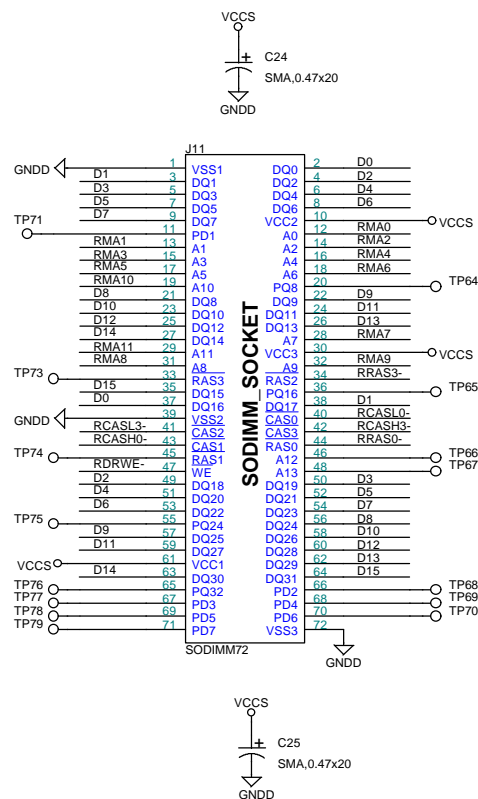
AEN AEN

IOR- IOR-  
IOW- IOW-

SMEMR- SMEMR-  
SMEMW- SMEMW-

RESETDRV RESETDRV





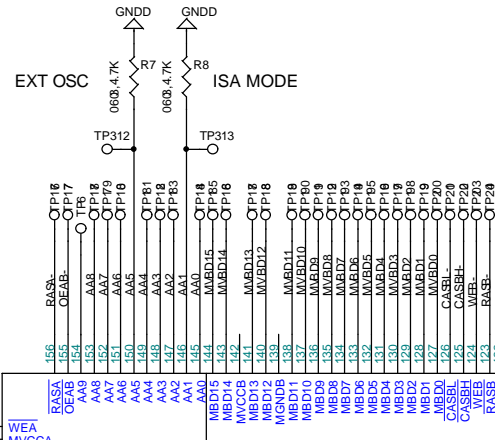
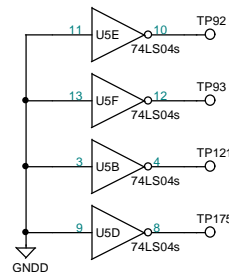
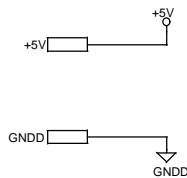
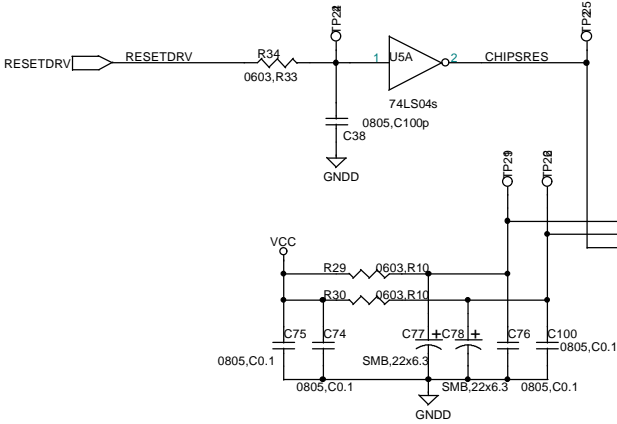
LA[17:23] I A[17:23]  
SA[0:16] SA[0:16]  
SD[0:15] SD[0:15]

IOCHRDY IOCHRDY  
IOCS16 IOCS16  
MEMCS16 MEMCS16

AEN AEN  
BALE BALE  
IOR- IOR-  
IOW- IOW-

MEMR- MEMR-  
MEMW- MEMW-  
REFRESH- REFRESH-

SBHE- SBHE-  
OSC OSC



DRAM "A"  
Display Memory  
Lower 512KB

DRAM "B"  
Display Memory  
Upper 512KB

DRAM "C"  
Frame Buffer  
or  
24-Bit  
PC-Video  
Interface

## 65545 Flat Panel VGA Controller

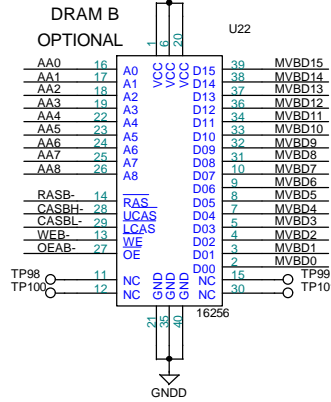
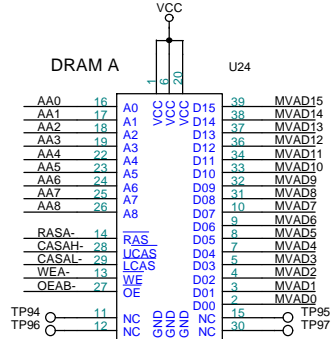
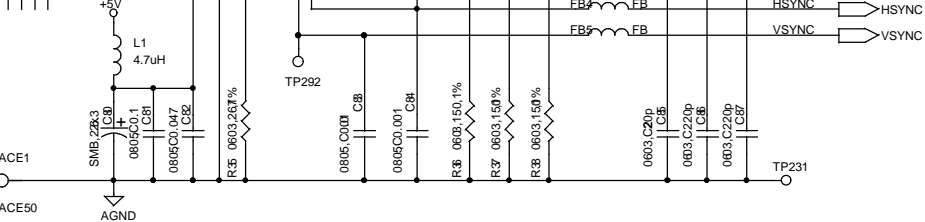
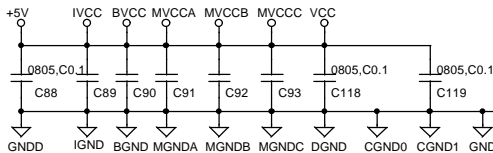
Configuration Pins  
2X# = 0 2X LCLK  
OS# = 0 External Oscillator (1=Xtal)  
AD# = 0 ENABKL & ACT1 are A26,A27  
TS# = 0 Enable Clock Test Mode  
LV# = 0 Input Threshold Level Control

Bus  
Interface  
Group

Clock  
Group

Bus  
Interface  
Group

DAC  
Group



PANEL\_INTERFACE

VGA